REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants observe that they have cancelled method Claims 37-68. Applicants further observe that structure Claims 2, 8-10, 15-28 and 33-36, which have been withdrawn by the Examiner, are not cancelled herein since applicants hope to have the non-elected species rejoined with Claims 1, 3-7, 11-14 and 29-32, which are pending in this application. No amendments have been made to pending Claims 3-7, 11-14 and 29-32. Claim 1, however, has been amended to emphasize that *a bonding interface is present between the semiconducting or non-semi-conducting substrate and the buried insulator layer*. Support for this amendment to Claim 1 is found in the present application at paragraph [0600]-paragraph [0671], particularly see FIG. 16 and lines 5-8 of paragraph [0690]. Applicants observe that in the above identified text the buried insulator is bonded to the semiconducting or non-semiconducting substrate and, as such, a bonding interface would exist between those two layers.

Since the above amendment to Claim 1 does not introduce new matter into the specification of the present application, entry thereof is respectfully requested.

In the present Office Action, the drawings have been objected under 37 C.F.R. § 1.83(a) as allegedly not showing each and every feature of the claims. Specifically, the limitation of Claim 5 that the substrate may "comprise strained layers, unstrained layers or a combination thereof" is allegedly not shown in the drawings.

Applicants respectfully disagree and submit that no changes to the drawings are necessary since region 12 was meant to include a semiconductor that can include stained layers, unstrained layers or a combination thereof. See paragraph [0034] of the originally filed

application. Applicants submit that when a combination of strained and unstrained layers are used region 12 would be a stack including the various layers. In view of the above remarks, applicants respectfully submit that the drawing object is improper and that the same can and should be withdrawn.

Claims 1, 3, 4, 5, 11, 12 and 14 stand rejected under 35 U.S.C. § 102(a) as allegedly anticipated by U.S. Patent No. 6,633,066 to Bae, et al. ("Bae, et al."). Claims 1, 3, 4, 6, 7, 11 and 12 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,906,951 to Chu, et al. ("Chu, et al."). Claims 1, 3, 4, 6, 7, 11, 12, 13 and 19-32 stand rejected under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent No. 6,677,655 to Fitzergald, et al. ("Fitzergald, et al.").

Concerning the § 102 rejections, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that the claims of the present application are not anticipated by the disclosure of Bae, et al. since the applied reference does not disclose applicants' claimed structure in which a bonding interface is present between a semiconducting or non-semiconducting substrate and a buried insulator layer, as presently claimed.

Bae, et al. disclose a method and structure consisting of an epitaxial Si (14)/SiGe (16)/Si (18) tri-layer film that is bonded and transferred to an oxide (22) located on the surface of a

supporting substrate (20). This process is illustrated in FIGS 3A-3E or 4A-4E of the applied reference. There are several differences between the method of Bae, et al. and the current application that lead to structural differences.

First, Bae, et al. transfer layers Si (14)/SiGe (16)/Si (18) onto an oxide 22. As a result, the bonding interface in the prior art structure is that between the oxide 22 and the Si film 18. The bonding interface of the prior art can contain many dangling bonds and defects, which translate into electronic states (traps) that may hold charge. It is therefore desirable to distance the bonding interface from the "device layers" so that any charge trapped at the bonding interface will not disturb the devices operation built into the device layers. The instant application discloses the transfer of a Ge-containing layer 18 (device layer), an adhesion layer 16 and a buried insulator 14 onto a semiconducting or non-semiconducting substrate 12. See, FIGS. 16 and 17 of the present application. The bonding interface in the present invention is therefore between the buried insulator 14 and the substrate 12. In other words, the bonding interface is offset by the full thickness of the buried insulator 14 from the Ge-containing device layer 18.

A second difference between Bae, et al and the present application is that the prior art uses epitaxy to form the Ge containing layer (layer 16, SiGe-epi). Due to the lattice mismatch between Si and SiGe it is only possible to grow relatively thin SiGe layer having a low content of Ge over Si without introducing dislocations. For example, the maximum typical thickness of a $Si_{1-x}Ge_x$ (x=0.2) film is about 200-300 nm before dislocations nucleate. For pure Ge (x=1.0), it is not possible to grow the Ge layer without dislocations. The presence of dislocation in the device layer can lead to device failure and potential reliability issues and therefore should be avoided. In the current application, the Ge-containing layer 18 is not formed by epitaxy, but is transferred from a donating Ge-containing substrate. As a result, the layer has the crystalline quality of the donating substrate and should be dislocation free.

In view of the above remarks, the anticipation rejection based on the disclosure of Bae, et al. has been obviated. Applicants thus respectfully request reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(a) citing Bae, et al.

Concerning the anticipation rejection citing Chu, et al., applicants respectfully submit that the claims of the present application are not anticipated by the disclosure of Chu, et al. since the applied reference does not disclose applicants' claimed structure in which a bonding interface is present between a semiconducting or non-semiconducting substrate and a buried insulator layer, as presently claimed.

Chu, et al. provide an SOI substrate and a method of fabricating the same. In accordance with the disclosure of Chu, et al., strained layers of Si and/or SiGe are first formed on a first substrate. Next, a layer of Si and/or SiO_2 is formed over the strained layers. A second substrate having an insulating layer on its upper surface is then bonded to the Si or SiO_2 layer that is present in the first substrate. Thereafter, the first substrate is removed.

As with Bae, et al., Chu, et al. disclose a structure in which the bonding interface is located between the buried insulator layer of the second substrate, e.g., layer 28, and layer 19 which may include Si or SiO_2. In the prior art structure, the bonding interface can again contain many dangling bonds and defects, which translate into electronic states (traps) that may hold charge. In contrast to Chu, et al., the bonding interface in the claimed structure is between the buried insulator 14 and the substrate 12. In other words, the bonding interface is offset by the full thickness of the buried insulator 14 from the Ge-containing device layer 18.

Applicants also observe that in Chu, et al., the Ge-containing layer is formed by epitaxy and as such, the above comments made in regard to Bae, et al. regarding the difference between an epitaxy grown Ge-containing layer and a non-epitaxially grown Ge-containing layer apply here as well.

In view of the above remarks, the anticipation rejection based on the disclosure of Chu, et al. has been obviated. Applicants thus respectfully request reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b) citing Chu, et al.

With respect to Fitzergald, applicants respectfully submit that the claims of the present application are not anticipated by the disclosure of Fitzergald. since the applied reference does not disclose applicants' claimed structure in which a bonding interface is present between a semiconducting or non-semiconducting substrate and a buried insulator layer, as presently claimed.

In accordance with Fitzergald, the Ge-containing layer is formed by epitaxy. Starting with a silicon substrate 304, a graded layer 0-100% Ge 300 is epitaxially grown on the substrate. The grading in the Ge content helps in reducing the dislocations and roughness. Yet when the Ge layer 302 is grown epitaxially on layer 300, it is still required to use chemical mechanical polishing (see Col. 3 lines 35-42) to reduce roughness (the roughness is a result of surface steps formed by dislocations). As explained above, in the present application the Ge-containing layer is transferred from a Ge substrate and thus devoid having defects. In Fitzergald, the Ge-containing film stack (layers 306, 302, and 300) is bonded to an oxide 310. As a result, the bonding interface is adjacent to the device layers. This is opposite to that of the present invention where the bonding interface is separated from the Ge-containing layer by the full thickness of the buried insulator layer.

In view of the above remarks, the anticipation rejection based on the disclosure of Fitzergald has been obviated. Applicants thus respectfully request reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(e) citing Fitzergald

The foregoing remarks clearly demonstrate that the applied references do not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore

the claims of the present application are not anticipated by the disclosures of Bae, et al., Chu, et al. and Fitzergald. Applicants respectfully submit that the instant § 102 rejections have been obviated and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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